

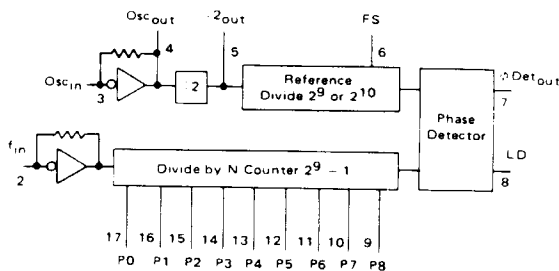
PLL FREQUENCY SYNTHESIZER

The MC145106 is a phase locked loop (PLL) frequency synthesizer constructed in CMOS on a single monolithic structure. This synthesizer finds applications in such areas as CB and FM transceivers. The device contains an oscillator/amplifier, a 210 or 211 divider chain for the oscillator signal, a programmable divider chain for the input signal and a phase detector. The MC145106 has circuitry for a 10.24 MHz oscillator or may operate with an external signal. The circuit provides a 5.12 MHz output signal, which can be used for frequency tripling. A 29 programmable divider divides the input signal frequency for channel selection. The inputs to the programmable divider are standard ground-to-supply binary signals. Pull-down resistors on these inputs normally set these inputs to ground enabling these programmable inputs to be controlled from a mechanical switch or electronic circuitry.

The phase detector may control a VCO and yields a high level signal when input frequency is low, and a low level signal when input frequency is high. An out of lock signal is provided from the on-chip lock detector with a "0" level for the out of lock condition.

- Single Power Supply
- Wide Supply Range: 4.5 to 12 V
- Provision for 10.24 MHz Crystal Oscillator
- 5.12 MHz Output
- Programmable Division Binary Input Selects up to 2^9
- On-Chip Pull Down Resistors on Programmable Divider Inputs
- Selectable Reference Divider, 2^{10} or 2^{11} (including -2)
- Three-State Phase Detector
- Pin-for-Pin Replacement for MM55106, MM55116
- Chip Complexity: 880 FETs or 220 Equivalent Gates

BLOCK DIAGRAM

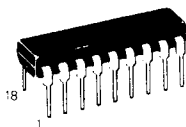


V_{DD} Pin 1
V_{SS} Pin 18

CMOS MSI

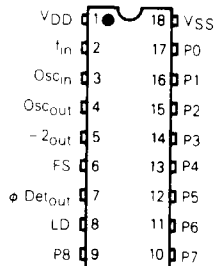
(LOW-POWER COMPLEMENTARY MOS)

PLL FREQUENCY SYNTHESIZER



P SUFFIX
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENT



MC145106

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +12	V
Input Voltage, All Inputs	V_{in}	-0.5 to $V_{DD} + 0.5$	V
DC Input Current, per Pin	I_{in}	± 10	mA
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

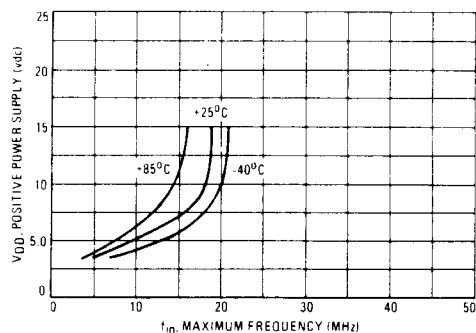
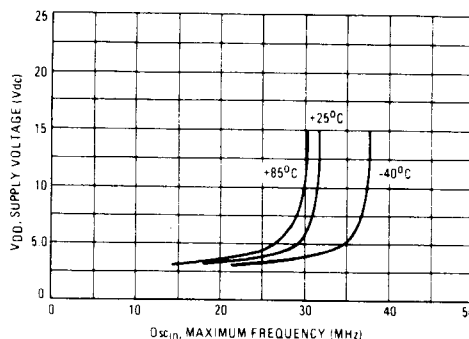
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq V_{in}$ or $V_{out} \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ Unless Otherwise Stated, Voltages Referenced to V_{SS})

Characteristic	Symbol	VDD Vdc	All Types			Unit
			Min	Typ	Max	
Power Supply Voltage Range	VDD	—	4.5	—	12	V
Supply Current	IDD	5.0 10 12	— — —	6 20 28	10 35 50	mA
Input Voltage	"0" Level "1" Level	VIL VIH	5.0 10 12	— — —	1.5 3.0 3.6	V
Input Current (IFS, Pull-up Resistor Source Current) (IP0 to P8) (IFS) (IP0 to P8, Pull-down Resistor Sink Current) (IOscin, fin) (IOscin, fin)	"0" Level "1" Level "0" Level "1" Level	Iin 				

TYPICAL CHARACTERISTICS

FIGURE 1 – MAXIMUM DIVIDER INPUT
FREQUENCY versus SUPPLY VOLTAGEFIGURE 2 – MAXIMUM OSCILLATOR INPUT
FREQUENCY versus SUPPLY VOLTAGE

TRUTH TABLE

Selection									Divide By N
P8	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	0	0	0	0	0	2 (Note 1)
0	0	0	0	0	0	0	0	1	3 (Note 1)
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
0	0	0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0	1	1	1	1	1	1	1	1	255
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	511

1: Voltage level = V_{DD}

0: Voltage level = 0 or open circuit input

Note 1: The binary setting of 00000000 and 00000001 on P8 to P0 results in a 2 and 3 division which is not in the 2^N-1 sequence. When pin is not connected the logic signal on that pin can be treated as a "0".

PIN DESCRIPTIONS

P0 – P8 – Programmable divider inputs (binary)

 f_{in} – Frequency input to programmable divider (derived from VCO)Osc_{in} – Oscillator/amplifier input terminalOsc_{out} – Oscillator/amplifier output terminal

LD – Lock detector, high when loop is locked, pulses low when out of lock.

ϕ Det_{out} – Signal for control of external VCO, output high when f_{in}/N is less than the reference frequency; output low when f_{in}/N is greater than the reference frequency. Reference frequency is the divided down oscillator input frequency typically 5.0 or 10 kHz.

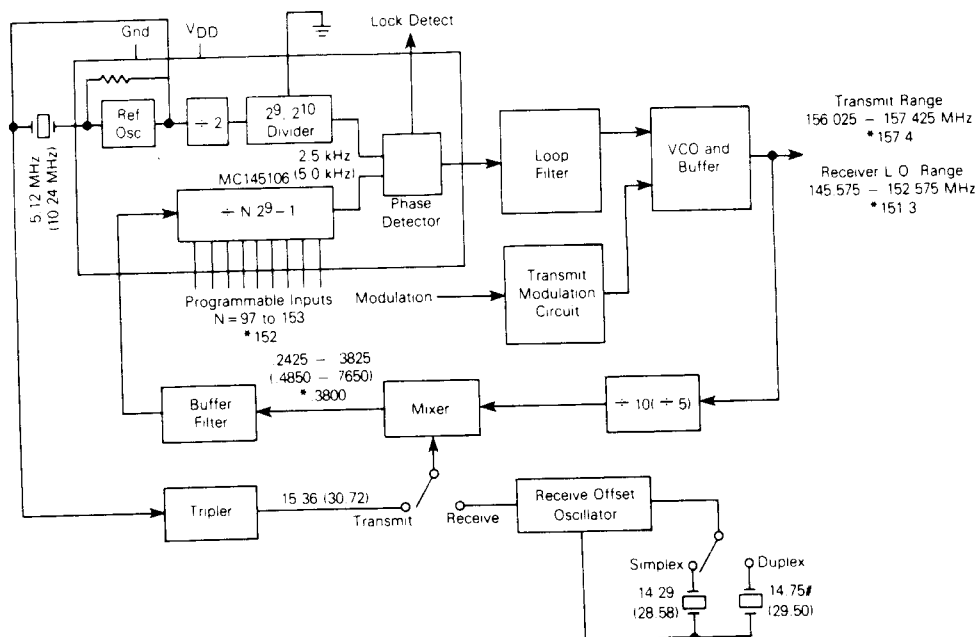
FS – Reference Oscillator Frequency Division Select. When using 10.24 MHz Osc frequency, this control selects 10 kHz, a "0" selects 5.0 kHz.

$\div 2_{out}$ – Reference Osc frequency divided by 2 output; when using 10.24 MHz Osc frequency, this output is 5.12 MHz for frequency tripling applications.

 V_{DD} – Positive power supply V_{SS} – Ground

MC145106

FIGURE 4 — VHF MARINE TRANSCEIVER SYNTHESIZER



NOTES:

- Receiver IF = 10.7 MHz
- Low Side Injection
- Duplex Offset = 4.6 MHz
- Step Size = 25 kHz
- Frequencies in MHz unless noted
- Values in Parentheses are for a 5.0 kHz Reference Frequency
- Example Frequencies for Channel 28 Shown by *
- Can be eliminated by adding 184 to $\pm N$ for Duplex Channels

MC145106

FIGURE 5 - VHF AIRCRAFT 720 CHANNEL TWO CRYSTAL FREQUENCY SYNTHESIZER

